ABSTRACT OF THE DISCLOSURE

A device structure and method for a non-volatile semiconductor device comprises a trenched floating gate and a control gate and further includes a source region, a drain region, a channel region, and an inter-gate dielectric layer. The trenched floating gate is formed in a trench etched into the semiconductor substrate. The trenched floating gate has a top surface which is substantially planar with a top surface of the substrate. The source and drain region have a depth approximately equal to or greater than the depth of the trench and partially extend laterally underneath the bottom of the trench. The inter-gate dielectric layer is formed on the top surface of the trenched floating gate, and the control gate is formed on the inter-gate dielectric layer. In one embodiment, the device structure also includes sidewall dopings that are implanted regions formed in the semiconductor substrate which extend substantially vertically along the length of the trench. The sidewall dopings are immediately contiguous the vertical sides of the trench and laterally separate the trench from the source region and the drain region.